WHAT IS CLAIMED IS:

1. A memory cell comprising:

a memory device having a set of memory ports, each memory port adapted to access to the memory device;

an address register having a plurality of sets of address lines, each set of address lines adapted to communicate a memory address with one of the set of memory ports; and

a memory partitioning set including at least one memory partitioning circuit, wherein the memory partitioning circuit is connected between an address line of one of the sets of address lines and a corresponding input of one of the set of memory ports, and wherein the memory partitioning circuit includes a first operation mode adapted to hold the corresponding input of one of the set of memory ports to a fixed value and a second operation mode adapted to pass the value of the connected address line to the corresponding input of one of the set of memory ports.

2. The memory cell of claim 1, wherein the memory partitioning set further comprises:

a first memory partitioning circuit connected with a first address line of the address register and an input of a first memory port of the memory device;

a second memory partitioning circuit connected with a second address line of the address register and an input of a second memory port of the memory device; and

wherein the first and second memory partitioning circuits are adapted to hold the inputs of their respective memory ports of the memory device to complementary values, thereby dividing the memory device into at least two single port memory partitions.

3. The memory cell of claim 1, wherein at least one memory partitioning circuit of the memory partitioning set includes a third operation mode adapted to invert the value of an address line of one of the sets of address lines.

4. The memory cell of claim 1, wherein at least one of the memory partitioning circuits of the memory partitioning set is responsive to a programmable device configuration specifying the mode of operation of the memory partitioning circuit.

5. The memory cell of claim 1, wherein at least one memory partitioning circuit is comprised of at least one multiplexer and an inverter gate.

6. The memory cell of claim 1, wherein the multiple port memory device is a two port RAM device.

7. A programmable device comprising:

a plurality of logic cells each adapted to perform a logic operation specified by a programmable device configuration;

a configuration memory adapted to store a programmable device configuration; and

at least one memory cell comprising:

a memory device having a set of memory ports, each memory port adapted to access to the memory device;

an address register having a plurality of sets of address lines, each set of address lines adapted to communicate a memory address with one of the set of memory ports; and

a memory partitioning set of at least one memory partitioning circuit connected between an address line of one of the sets of address lines and a corresponding input of one of the set of memory ports, wherein the memory partitioning circuit includes a first operation mode adapted to hold the corresponding input of one of the set of memory ports to a fixed value and a second mode of operation adapted to pass the value of the connected address line to the corresponding input of one of the set of memory ports.

8. The programmable device of claim 7, wherein the memory partitioning set further comprises:

a first memory partitioning circuit connected with a first address line of the address register and an input of a first memory port of the memory device;

a second memory partitioning circuit connected with a second address line of the address register and an input of a second memory port of the memory device; and

wherein the first and second memory partitioning circuits are adapted to hold the inputs of their respective memory ports of the memory device to complementary values, thereby dividing the memory device into at least two single port memory partitions.

9. The programmable device of claim 7, wherein at least one memory partitioning circuit of the memory partitioning set includes a third operation mode adapted to invert the value of an address line of one of the sets of address lines.

10. The programmable device of claim 7, wherein at least one of the memory partitioning circuits of the memory partitioning set is responsive to a programmable device configuration specifying the mode of operation of the memory partitioning circuit.

11. The programmable device of claim 7, wherein at least one memory partitioning circuit is comprised of at least one multiplexer and an inverter gate.

12. The programmable device of claim 7, wherein the multiple port memory device is a two port RAM device.

13. A system having a plurality of devices, the system comprising:

a non-volatile memory device storing a programmable device configuration;

a programmable device connected with the non-volatile memory device, the programmable device comprising:

a plurality of logic cells each adapted to perform a logic operation specified by a programmable device configuration;

a configuration memory adapted to store a programmable device configuration received from the non-volatile memory device; and

at least one memory cell comprising:

a memory device having a set of memory ports, each memory port adapted to access to the memory device;

an address register having a plurality of sets of address lines, each set of address lines adapted to communicate a memory address with one of the set of memory ports; and

a memory partitioning set of at least one memory partitioning circuit connected between an address line of one of the sets of address lines and a corresponding input of one of the set of memory ports, wherein the memory partitioning circuit includes a first operation mode adapted to hold the corresponding input of one of the set of memory ports to a fixed value and a second mode of operation adapted to pass the value of the connected address line to the corresponding input of one of the set of memory ports.

14. The system of claim 13, wherein the memory partitioning set further comprises:

a first memory partitioning circuit connected with a first address line of the address register and an input of a first memory port of the memory device;

a second memory partitioning circuit connected with a second address line of the address register and an input of a second memory port of the memory device; and

wherein the first and second memory partitioning circuits are adapted to hold the inputs of their respective memory ports of the memory device to complementary values, thereby dividing the memory device into at least two single port memory partitions.

15. The system of claim 13, wherein at least one memory partitioning circuit of the memory partitioning set includes a third operation mode adapted to invert the value of an address line of one of the sets of address lines.

16. The system of claim 13, wherein at least one of the memory partitioning circuits of the memory partitioning set is responsive to a programmable device configuration specifying the mode of operation of the memory partitioning circuit.

17. The system of claim 13, wherein at least one memory partitioning circuit is comprised of at least one multiplexer and an inverter gate.

18. The system of claim 13, wherein the multiple port memory device is a two port RAM device.

19. An information storage medium including a device configuration specifying a configuration of a programmable device, the device configuration comprising:

a first portion adapted to configure a plurality of logic cells of a programmable device to perform a plurality of logic operations;

a second portion adapted to configure a reconfigurable switching circuit of the programmable device to selectively route data connections between the plurality of logic cells; and

a third portion adapted to configure a set of memory partitioning circuits associated with a memory cell of the programmable device, wherein each of the set of memory partitioning circuits has a first operation mode adapted to hold an input of a first memory port of a multiple port memory device of the memory cell to a fixed value and a

second operation mode adapted to pass a value of an address line to the input of a first memory port of a multiple port memory device of the memory cell.

20. The information storage medium of claim 19, wherein the set of memory partitioning circuits includes:

a first memory partitioning circuit connected with a first address line of the address register and an input of a first memory port of the memory device; and

a second memory partitioning circuit connected with a second address line of the address register and an input of a second memory port of the memory device;

and wherein the third portion of the device configuration is adapted to configure the first and second memory partitioning circuits to hold the inputs of their respective memory ports of the memory device to complementary values, thereby dividing the multiple port memory device into at least two single port memory partitions.

21. The information storage medium of claim 19, wherein at least one memory partitioning circuit of the set of memory partitioning circuits includes a third operation mode adapted to invert the value of an address line of one of the sets of address lines.

22. The information storage medium of claim 19, wherein at least one memory partitioning circuit is comprised of at least one multiplexer and an inverter gate.

23. The information storage medium of claim 19, wherein the multiple port memory device is a two port RAM device.